MULTI-STAGE
NUMERIC COUNTER OSCILLATOR

FIELD OF THE INVENTION

The invention relates generally to automatic test equipment, and more particularly high accuracy digital counter circuits.

BACKGROUND OF THE INVENTION

Numerical counter oscillators (NCO), or accumulators, are convenient multi-bit registers that increment a summed value in response to a periodic input signal, such as a digital clock waveform. One application for an NCO is in a technique known as direct-digital-synthesis, often used to generate a variable frequency clock. Direct-digital-synthesis (DDS) for generating variable frequency clocks are well-known in the art and, as shown in Figure 1, generally involve driving the input of an NCO 10 with a digital clock signal 12. The counter incrementally advances with each subsequent clock period.

Each multi-bit count value is mapped to a sine value look-up table or memory 14 for a digital representation of an analog sine wave phase angle. The digital representation is then fed through a digital-to-analog converter (DAC) 16 where the accumulating phase angle results in a complete sinusoidal analog waveform. Further conditioning of the analog signal by a filter 18 and a phase-locked-loop (PLL) 20 often occurs to form the desired clock.

Conventionally, the frequency of the desired end waveform typically relies on the accuracy of the NCO. The degree of accuracy is typically characterized by the equation $F_{NCO} = F_{ref}(A/B)$, where F_{NCO} is the desired frequency and Fref is the digital input clock frequency. The "A" and "B" terms together represent a ratio of Fref to F_{NCO}. The "B" term traditionally represents a binary divisor dependent on the number of output bits N in the NCO.

In other words, the ratio A/B forces a $1/2^N$ resolution when programming a desired clock frequency F_{NCO}. The resulting problem is that a user desiring to program a variable frequency clock to, for example, one gigahertz, because of the limited number of available values for "B", might have to accept a frequency of 1.001 gigahertz. In some applications, such as automatic test equipment, this level of inaccuracy is problematic.

What is needed and currently unavailable is an NCO that provides a high level of accuracy that correspondingly allows more flexibility in frequency resolution for variable frequency clock generators and other circuits that utilize NCOs. The NCO described herein satisfies these needs.

SUMMARY

The numeric counter oscillator described herein provides a unique way to achieve high accuracy and repeatability for circuits that use direct-digital-synthesis techniques.

To realize the foregoing advantages, the numeric counter oscillator in one form comprises a numeric counter oscillator comprising a quotient accumulator and a remainder accumulator. The quotient accumulator has a programmable input for receiving a QUOTIENT value, a reference clock input and a multi-bit output. The output is adapted for transmitting an output value OUT representing an accumulated quotient sum. The multi-bit output increments by a predetermined amount in response to each reference clock period. The remainder accumulator comprises programmable inputs for receiving respective REMAINDER and DIVISOR values, a a reference clock input and a multi-bit output representing an accumulated digital remainder sum less than a predefined digital integer. The remainder accumulator further comprises a comparator having a first input for receiving a programmed divisor value, and a second input for receiving the remainder accumulator multi-bit output. The comparator is operative to generate an increment carry signal for application to the quotient accumulator when the remainder multi-bit output reaches the predefined integer value.

Other features and advantages of the present invention will be apparent from the following detailed description when read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be better understood by reference to the following more detailed description and accompanying drawings in which

FIG. 1 is a high-level block diagram of a conventional circuit for generating a variable frequency clock;

FIG. 2 is a block diagram of an improved numerical counter oscillator;

FIG. 3 is a table showing various values at different points in the improved NCO of Figure 2 for each clock cycle; and

FIG. 4 is a high-level block diagram of a variable frequency clock generator employing the improved numeric counter oscillator of Figure 2.

DETAILED DESCRIPTION

The numeric counter oscillator (NCO) described herein provides a way to maximize the accuracy of an oscillator output with respect to a desired frequency ratio between two clock frequencies. This enables a flexible choice of resolution in the NCO output for use with a variable frequency clock, or timestamp as more fully described below.

Referring now to Figure 2, the multi-stage numerical counter oscillator, generally designated 30, comprises a quotient accumulator 40 and a remainder accumulator 50. The remainder accumulator complements the quotient accumulator to allow for flexible clock frequency resolution programming.

Further referring to Figure 2, the quotient accumulator includes a first adder 42 that receives at one input an eighteen-bit quotient value QUOTIENT, and an eightee-bit input fed back from the accumulator output OUT. The first adder feeds a second adder 44 with the result of the summed QUOTIENT and OUT values. The second adder sums the QUOTIENT/OUT with a carry input from the remainder accumulator 50. The output from the second adder is shifted into a multi-bit register 46 clocked by input clock CLK. The output of the register OUT may then be used as the accumulator input.

With continued reference to Figure 2, the remainder accumulator 50 includes a third adder 52 that receives a thirty-bit remainder input REMAINDER, along with an increment value from a second multi-bit register 54. The output of the third adder is fed as an input to a subtractor 56 and a comparator 58. A thirty-bit divisor value DIVISOR provides a second input for the subtractor and comparator. A multiplexer 60 includes a control input coupled to the comparator output to selectively pass the subtractor output or the third adder output to the second register 54.

Figure 3 illustrates a cycle-by-cycle example of how the multi-stage NCO operates. This example assumes a desired ratio between the desired frequency FNCO and the reference frequency FREF of 10/3. This assumption results in a programmed quotient of three (3), a remainder of one (1), and a divisor of three (3).

With the assumptions above as one example, at cycle zero (0), the remainder accumulator has an incremental value of zero, with the quotient accumulator output incremented by three (3). With cycle 1, the remainder accumulator increments by one (1), resulting in an adder output of two (2). The quotient accumulator increments by three (3) again, for an output value, at the adder , of six (6).

With continued reference to Figure 3, at cycle 2 (the third clock pulse), the adder input is incremented to generate a value of three (3) at the input to the subtractor and the comparator. Since both inputs to the comparator are equal, a carry signal is generated and fed to the quotient accumulator (the second adder input). The carry value is added with the incrementing three (3) on the fourth clock pulse. As a result, the output OUT exhibits a ten (10).

The entire carry-generation process repeats every three (3) cycles (the DIVISOR value) to produce an accurate counter output OUT. As a result, the resolution of the clock is programmable to a very fine resolution, for example, to one hertz. Of course, the QUOTIENT, REMAINDER, and DIVISOR input values are entirely programmable by a user in establishing the desired frequency ratio.

With reference now to Figure 4, the NCO 30 in one application may be conveniently employed in a variable frequency clock generator, generally designated 100, utilizing direct-digital-synthesis techniques well-known to those skilled in the art, and briefly described earlier herein. The NCO feeds its high-accuracy output to a look-up sine table 102 having amplitude values for phase input. Each accumulated amplitude value is then fed to a digital-to-analog converter (DAC) 104 where a stepped analog waveform results. The waveform is then smoothed and processed by a filter 106 and clipped by a clipper 107 to make a clock. Preferably, a phase-locked-loop 108 further filters the waveform for optimum fidelity.

In another application, and referring back to Figure 2, the NCO 30 may be employed as a standard circuit block to generate timestamp data. Timestamps are often useful for establishing relative timings between signal occurances or events. For this application, both of the accumulator outputs are used such that the quotient accumulator output represents integers of a specified unit of time, such as nanoseconds.

Those skilled in the art will recognize the many benefits and advantages afforded by the present invention. Of significant importance is the dual accumulator aspect of the NCO, which enables the quotient to be regularly corrected during operation. This allows for a high degree of resolution flexibility for applications such as variable frequency waveform generation and timestamping.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention.